

## Silicon N-Channel SGT Power MOSFET

### Description

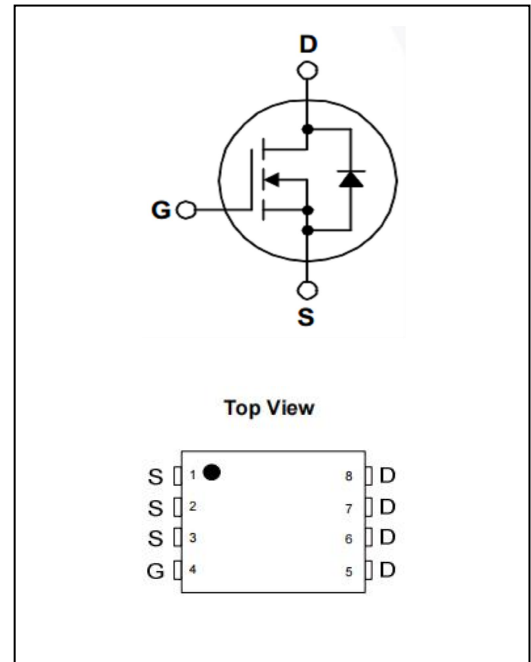
The TH043N06GDFN uses advanced split gate trench technology to achieve extremely low Static Drain-to-Source on-Resistance  $R_{DS(on)}$ . It can be used in a wide variety of applications.

### General Features

- $V_{DS}=60V$ ,  $R_{dson} \leq 4.3m\Omega$  @  $V_{GS}=10V$ ,  $I_D=20A$  (Typ:  $3.8m\Omega$ )
- Low ON Resistance ( $R_{dson} \leq 4.3m\Omega$ )
- Low Reverse transfer capacitance
- 100% Single Pulse avalanche energy Test

### Application

- E-Bike Controller Applications
- Power switching application
- Load switch



### Electrical Characteristics @ $T_a=25^\circ C$ (unless otherwise specified)

#### a) Limited Parameters:

Symbol	Parameter	Value	Units
$V_{DSS}$	Drain-to-Source Breakdown Voltage	60	V
$I_D$	Drain Current (continuous) at $T_c=25^\circ C$	140	A
	Drain Current (continuous) at $T_c=100^\circ C$	98	A
$I_{DM}$	Drain Current (Pulsed)	420	A
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$P_{tot}$	Total Dissipation at $T_c=25^\circ C$	180	W
$T_j$	Max. Operating Junction Temperature	-55 to 175	$^\circ C$
Eas	Single Pulse Avalanche Energy	390	mJ

**b) Electrical Parameters:**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{DS}$	Drain-source Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
$R_{DS(on)}$	Static Drain-to-Source on-Resistance	$V_{GS}=10V, I_D=20A$		3.8	4.3	m $\Omega$
$V_{GS(th)}$	Gated Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1.0	$\mu A$
$I_{GSS(F)}$	Gated Body Leakage Current	$V_{GS}=+20V,$			100	nA
$I_{GSS(R)}$	Gated Body Leakage Current	$V_{GS}=-20V,$			-100	nA
$C_{iss}$	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=50V,$ $f=1.0MHz$		3856		pF
$C_{oss}$	Output Capacitance			1230		pF
$C_{rss}$	Reverse Transfer Capacitance			82		pF
$Q_g$	Total Gate Charge	$V_{DS}=40V,$ $I_D=50A,$ $V_{GS}=10V,$ $f=1.0MHz$		72		nC
$Q_{gs}$	Gate-Source Charge			302		nC
$Q_{gd}$	Gate-Drain Charge			13		nC
$R_g$	Total Gate Resistance			1.2		$\Omega$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{d(on)}$	Turn-on Delay Time	$V_{DS}=40V,$ $I_D=50A,$ $V_{GS}=10V,$ $R_g=3.0\Omega,$		25		nS
$T_r$	Turn-on Rise Time			22		nS
$T_{d(off)}$	Turn-off Delay Time			51		nS
$T_f$	Turn-off Fall Time			29		nS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{SD}$	S-D Current (Body Diode)			140		A
$I_{SDM}$	Pulse S-D Current (Body Diode)			560		A
$V_{SD}$	Diode Forward Voltage	$V_{GS}=0V, I_{DS}=30A$			1.2	V
$T_{rr}$	Reverse Recovery Time	$T_j=25^\circ C, I_F=120A$ $di/dt=100A/\mu s$		52		nS
$Q_{rr}$	Reverse Recovery Charge			146		nC

\*Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$

Symbol	Parameter	Typ	Units
$R_{\theta JC}$	Junction-to-Case	0.68	$^\circ C/W$

Typical Characteristics

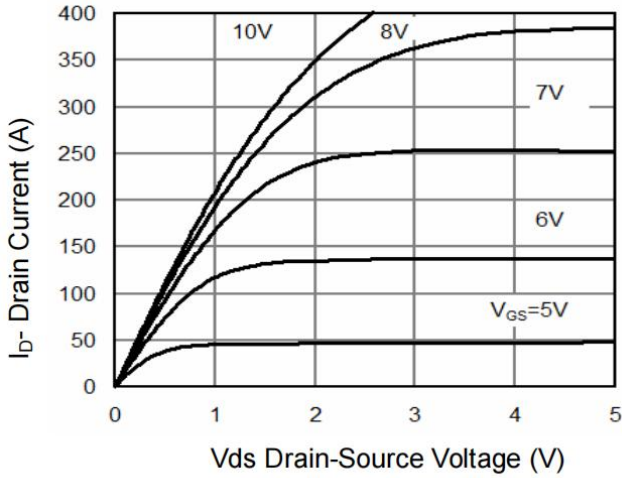


Figure 1 Output Characteristics

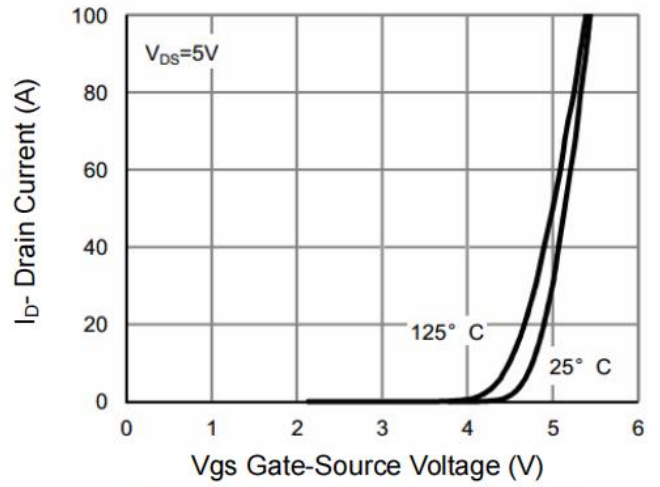


Figure 2 Transfer Characteristics

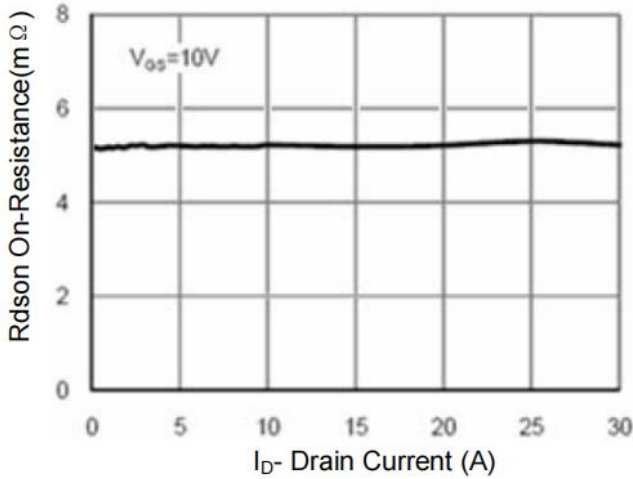


Figure 3 Rdson- Drain Current

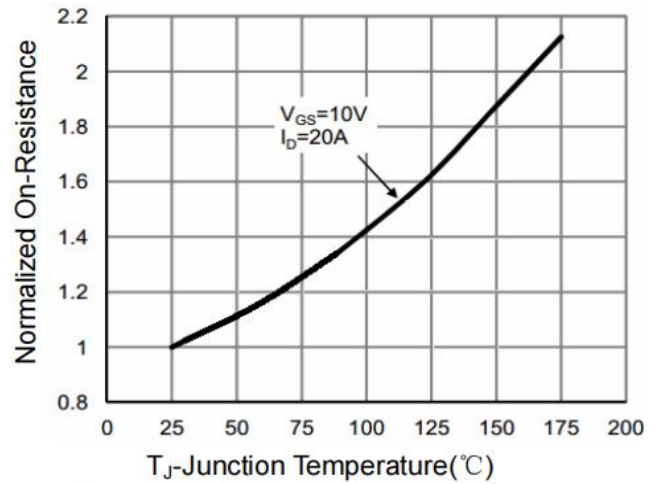


Figure 4 Rdson-Junction Temperature

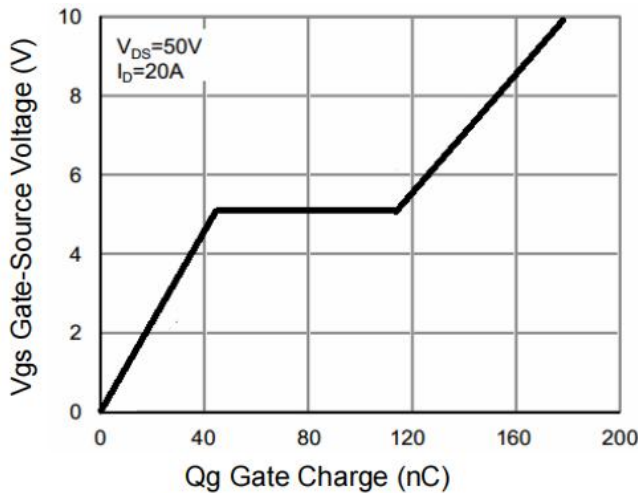


Figure 5 Gate Charge

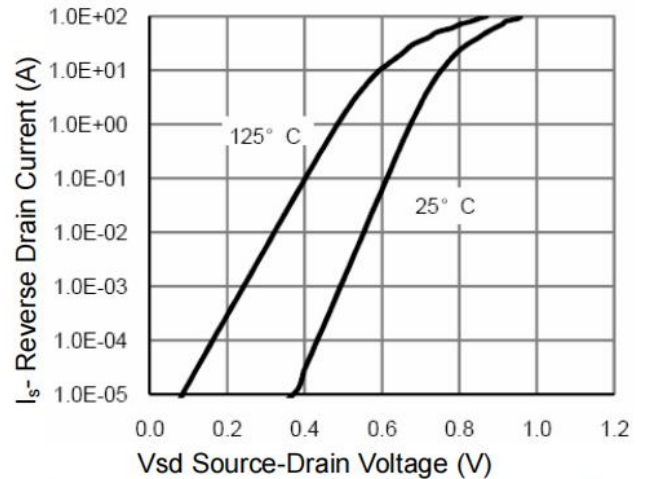


Figure 6 Source- Drain Diode Forward

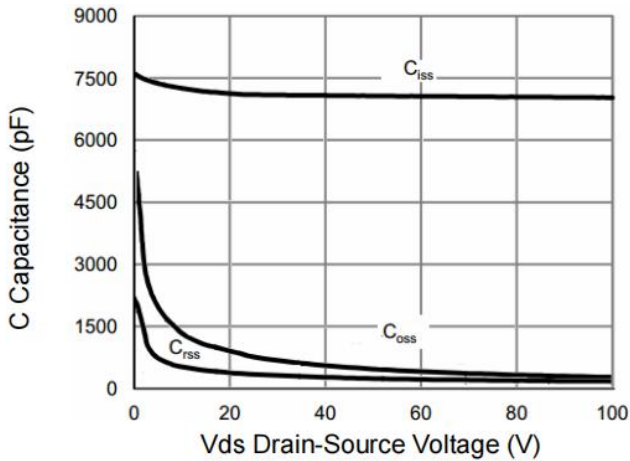


Figure 7 Capacitance vs Vds

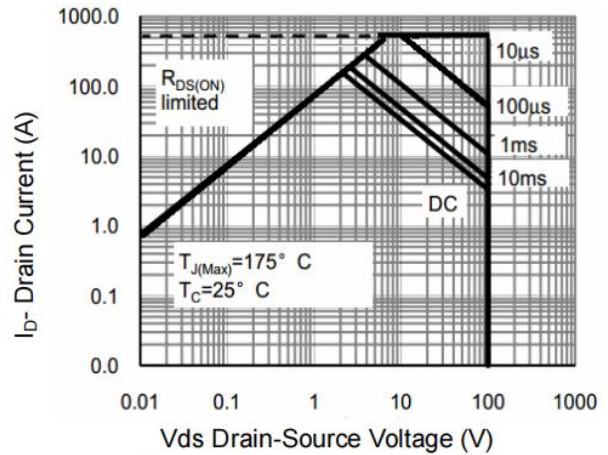


Figure 8 Safe Operation Area

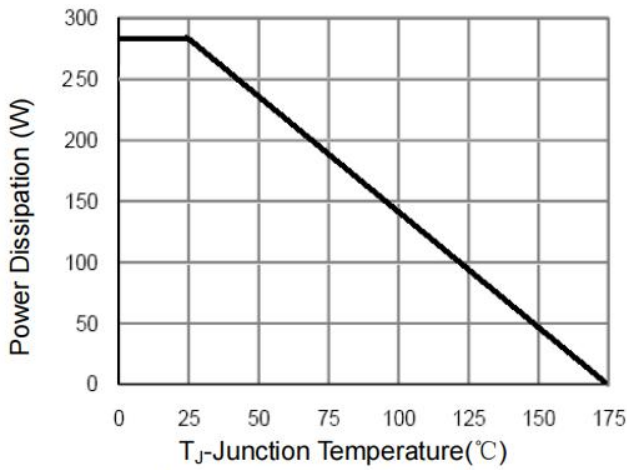


Figure 9 Power De-rating

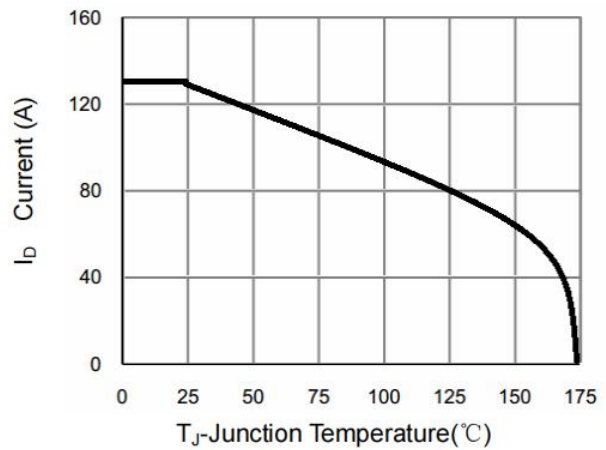


Figure 10 ID Current- Junction Temperature

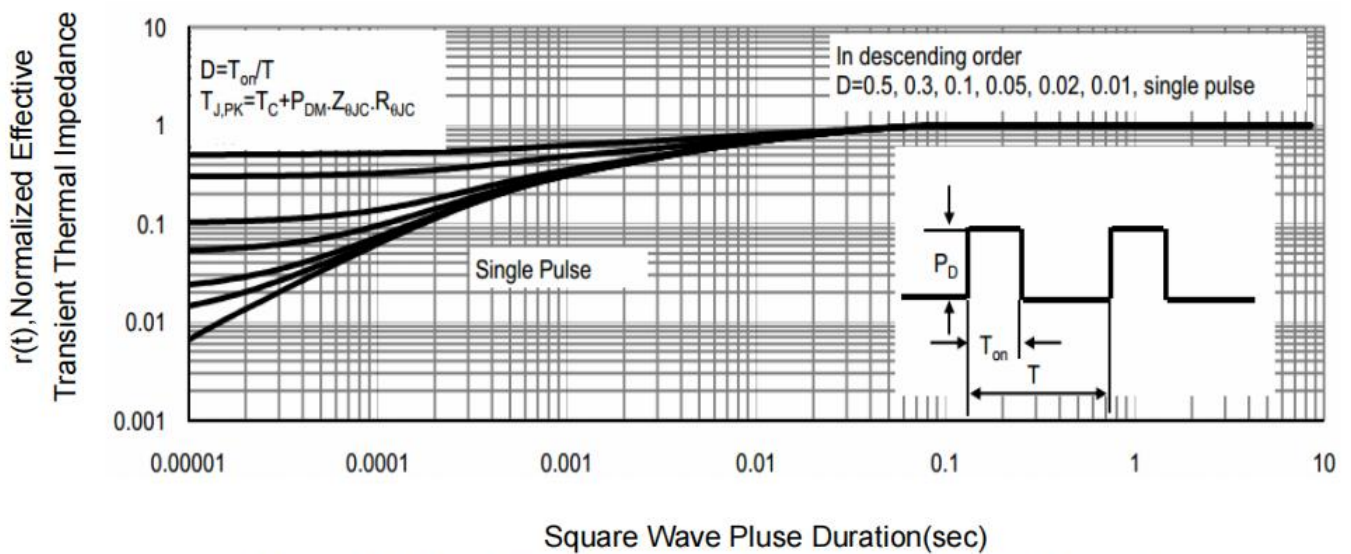
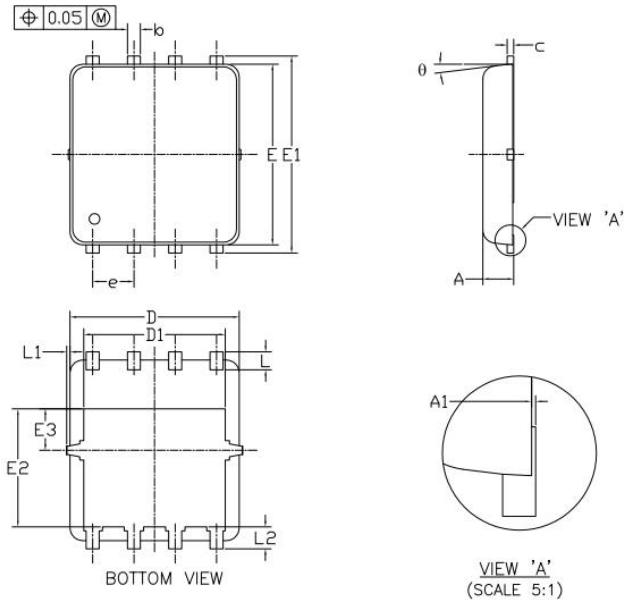


Figure 11 Normalized Maximum Transient Thermal Impedance

## Package Information

### DFN 5\*6 PACKAGE



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.95	1.00
A1	0.00	---	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	5.10	5.20	5.30
D1	4.25	4.35	4.45
E	5.45	5.55	5.65
E1	5.95	6.05	6.15
E2	3.525	3.625	3.725
E3	1.175	1.275	1.375
e	1.27 BSC		
L	0.45	0.55	0.65
L1	0	---	0.15
L2	0.68 REF		
θ	0°	---	10°

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